

Design and Implementation of Digital Timing Recovery and Carrier Synchronization for High Speed Wireless Communication

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As communication algorithms continue to increase in complexity, greater constraints are placed upon the hardware used to fully utilize the capabilities of these algorithms. These new algorithms attempt to achieve the highest possible bandwidth efficiency by utilizing diversity in time, frequency and space dimensions, leaving little room for error in synchronization systems. Furthermore, as more high bandwidth receivers become incorporated into small mobile devices, this high synchronizer performance must be attained at a low power cost as well. The driver for this project is the design of an indoor wireless communication system capable of high data rate downlink and multiple portable receivers. We will implement and test advanced timing recovery and carrier synchronization methods that move most of the computation to the digital back end, reducing power consumption.



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by Paul James Husted

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of Master of Science, Plan II.

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Abstract

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As communication algorithms continue to increase in complexity, greater constraints are placed upon the hardware used to fully utilize the capabilities of these algorithms. These new algorithms attempt to achieve the highest possible bandwidth efficiency by utilizing diversity in the time, frequency, and space dimensions, leaving little room for error in synchronization systems. Furthermore, as more high bandwidth receivers become incorporated into small mobile devices, this high synchronizer performance must be attained at a low power cost as well.

The driver for this project is the design of an indoor wireless communication system capable of high data rate downlink to multiple portable receivers. We will implement and test advanced timing recovery and carrier synchronization methods that move most of the computation to the digital back end, reducing power consumption. The use of a free-running digital sampling clock, unrelated to the symbol rate, will likewise reduce the overall chip complexity by removing voltage controlled oscillator circuitry from the

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analog front end. We will use a systematic design methodology to create a system which provides a synchronized, coherent signal for further digital baseband processing.

In addition to studying the analytical effects of this synchronization system, implementation details will also be discussed. A new design flow allowing push-button creation of silicon from a high-level simulation description will be discussed, including the constraints necessary upon the designer and the benefits of having a functional system-level simulation able to be translated directly to hardware.

As technology scaling continues to reduce feature size, the cost of additional digital processing to increase synchronization performance should be negligible. The performance benefit of the system will allow more complex algorithms to be implemented, allowing for higher bandwidth efficiency, and increased radio performance for each user.

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3.4 Carrier Offset Estimation and Fine Timing Synchronization

Once it is determined that the receiver has just received the first two PN sequences of the known pilot code, the rest of the pilot code is used to find the fine timing estimate and the carrier offset estimate. Again, since we are essentially subsampled at 25 MHz, our best resolution for fine timing will be to choose the optimal substream, and assume that this choice of sampling instant is the best that can be done. Using this substream, we can estimate the carrier offset, and use this estimate to correct the substream of choice so that its constellation is no longer rotating.

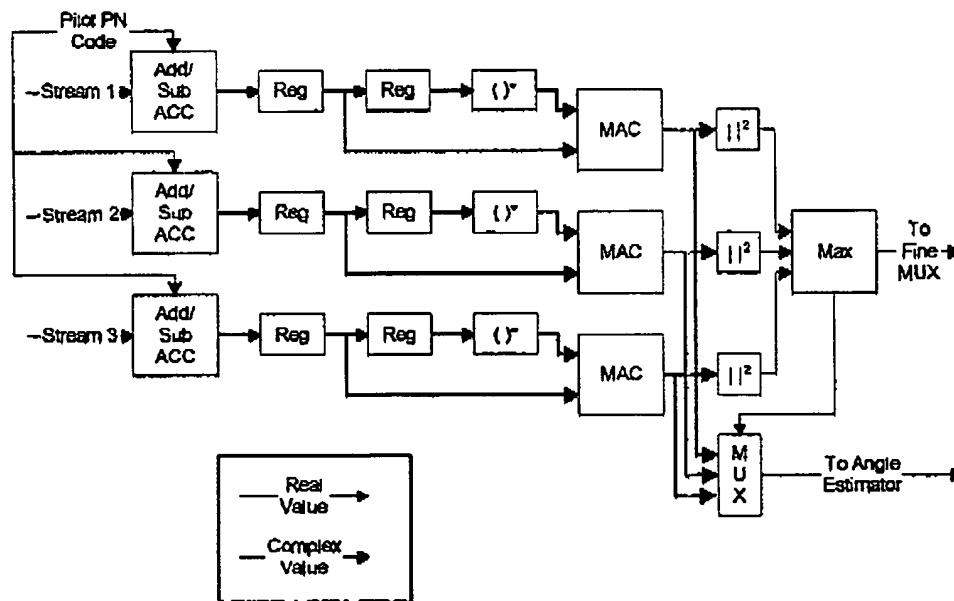


Figure 3-10 Fine Timing Synchronization and Carrier Offset Estimation

The coarse timing estimate chooses one of substreams 2, 4, or 7 as having the greatest squared magnitude of correlation peak, corresponding to a coarse estimate of the strongest power sampling point. Based on this coarse estimate, we will further evaluate

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the coarse stream estimate and its two immediate neighbors – in other words, we will evaluate three streams, a member of the set of substreams $\{\{1, 2, 3\}, \{3, 4, 5\}, \{6, 7, 8\}\}$. These sets are asymmetrical due to the availability of only 8 substreams from the ADC decimation filters. These substreams will be correlated with the pilot PN code, and the output will be put through a MAC to find a fine timing estimate according to the following formula [MMF98]:

$$\hat{\mu} = \arg \max_p \left| \sum_{i=1}^{L_{\text{cor}}} [z_i - z_i^* \dots] d_i \right|$$

The advantage of using correlation values rather than the chip values is due to the effect of multipath. Since there is no equalizer before the synchronization block for a frequency selective indoor channel, we must use the excellent autocorrelation properties of the PN code to reduce the effect of multipath on the values fed into our estimator.

This process involves simply multiplying each correlation sum with the complex conjugate of the preceding correlation sum. The maximum absolute value of this summation corresponds to the optimal substream to pass along to the correlator. The MAC thus only needs to run at the symbol rate rather than at the chip rate, greatly reducing the power consumption during pilot mode. Three MACs are necessary for this design, but it could be possible to time-multiplex these MACs with a MUD correlator. An adaptive correlator adapting to the data code would be idle during the pilot mode, so these MACs can be time multiplexed to reduce total area necessary on the chip.

As a bonus, from this same calculation we can also calculate the carrier offset estimate according to the following formula [MMF98]:

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$$\hat{\Omega}T = \arg \left\{ \sum_{l=1}^{L/M} [z_n - z^*_{n-1}] d_l \right\}_{l=\hat{\mu}}$$

By multiplying each correlation sum by the conjugate of the previous correlation sum, we get an estimate of the phase difference due to carrier offset between the two symbols.

The transmitter sends unmodulated symbols, so with no carrier offset they would be despread at the receiver to have the same phase, and multiplying a symbol by the previous symbol's conjugate would create a product with 0 mean angle. Inducing a carrier offset creates a non-zero mean phase difference between consecutive symbols, equal to the phase difference per symbol due to carrier offset. The equation above sums multiple products into a single phasor, and the angle of this phasor divided by the symbol length in chips is our phase difference per chip due to carrier offset. We can safely assume that the channel remains constant over the duration of the pilot symbol, so the channel effects will be constant for each PN symbol in the pilot duration, leading to a valid carrier offset estimate. The variance of this estimate can be calculated via the following equation [MMF98]:

$$\text{var}[\hat{\Omega}T] = \sigma_{\hat{\Omega}T}^2 = \frac{1}{D^2} \left(\frac{D}{L^2} \frac{2}{2E_s/N_0} + \frac{1}{L^2} \frac{2}{\left(2E_s/N_0\right)^2} \right)$$

where L is the number of correlation sums used in the estimation summation, and D is the separation in symbols of the compared values. For our application, we must restrict ourselves to using only D = 1. When using 50 ppm oscillators transmitting at 2 GHz, the maximum carrier offset is 200 kHz. For a symbol rate of about 800 kHz, using D = 2 could result in an estimate of phase difference between consecutive chips of greater than π , which will result in a phasor rotating in the incorrect direction.